Multi-Level Multi-Core Distributed Trace Synchronization

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Areas of study

- Multi-Core architectures characteristics
- Virtualization software and hardware support
- Multi-level Multi-core Distributed Trace Synchronization

Multi-Core architectures

- Clocks sharing and synchronization.
- Shared memory and Non Uniform Memory Access (NUMA).
- On chip high speed low latency networking
- Other inter processor synchronization and communication mechanisms.

Multi-Core architectures

- Intel : Teraflops Research Chip (Polaris)
  - 80 cores, each containing two engines and one 5-port router
  - 5.7 GHz
- AMD: Phenom processor
- IBM: Cell Micro processor
- Sun: Ultra SPARC-T2
- Tilera: TILE64

Virtualization

- Hardware support for Intel, AMD and PowerPC architectures
- Virtualization software (QEMU, KVM, XEN)
- Modeling the state of traced virtual and physical systems

Multi-level Multi-core Distributed Trace Synchronization

- Challenges of Distributed Systems
  - Different types of networking hardware and protocols
  - Clock synchronization
  - Dependency analysis across nodes
- Challenges of Multi-core systems
  - Very high throughput
  - Scalability
  - Clock synchronization